UNITRODE

Full Bridge Power Amplifier

FEATURES

- Plug-in Compatibility with the UC3173A
- 5V or 12V Operation
- 13mA Quiescent Supply Current
- 1.8mA Standby Current
- Precision Current Control
- ±1A Load Current
- 1.65V Typical Total VSAT at 1A
- Controlled Velocity Head Parking
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Bandwidth Control
- Inhibit Input and UVLO
- PLCC, SOIC, and Low Profile Quad Flat Pack Packages

DESCRIPTION

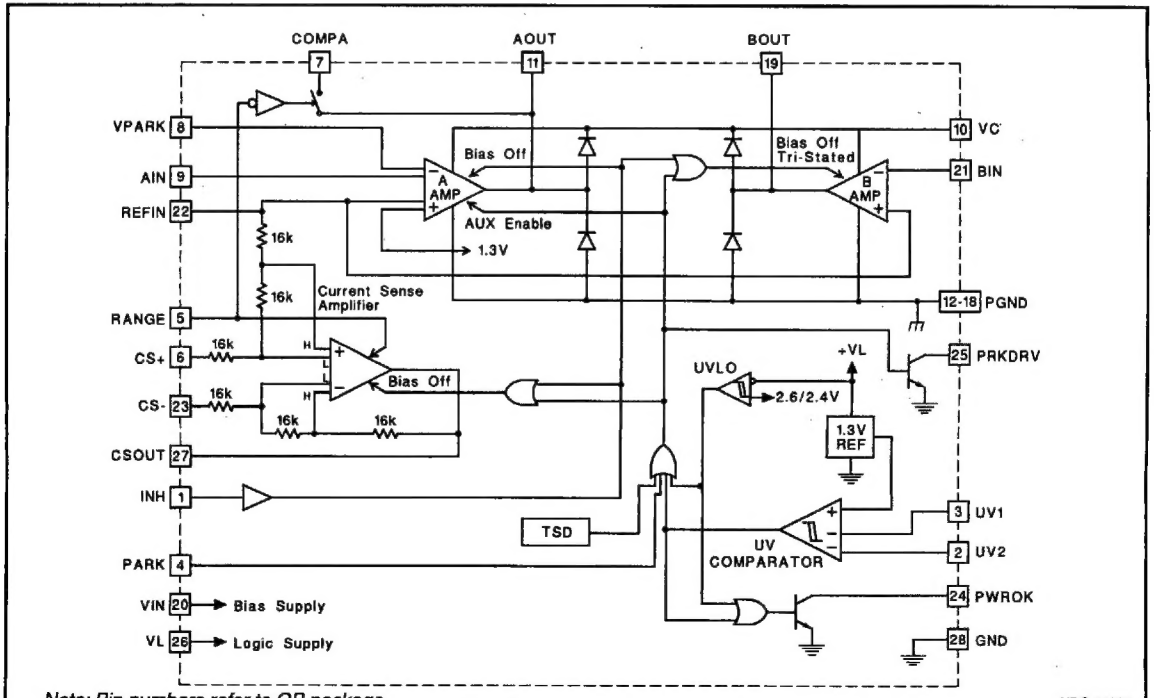
The UC3172A power amplifier is pin-for-pin compatible with the UC3173A. Improvements have been made to allow more liberal application of the device.

This full bridge power amplifier, rated for continuous output current of 1A, is intended for use in demanding servo applications such as head positioning for high-density disk drives. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3172A is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited the device will draw less than 1.8mA of total supply current.

Auxiliary functions on this device include a dual-input undervoltage comparator, which can monitor two independent supply voltages and activate the built- in head park function when either is below minimum. The park circuitry allows a programmable retract voltage to be applied to the load for limiting maximum head velocity. A separate low-side parking drive pin permits a series impedance to be inserted to control maximum retract current. The parking drive function can be configured to operate with supply voltages as low as 1.2V.

The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.

BLOCK DIAGRAM



Note: Pin numbers refer to QP package.

UDG-94039

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, (VIN, VC, VL) 18V
UV Comparator
  Maximum Forced Voltage ..... –0.3V to 6V
  Maximum Forced Current ..... ±10mA
Logic Inputs and REFIN
  Maximum Forced Voltage ..... –0.3V to 10V
  Maximum Forced Current ..... ±10mA
B Amplifier Inverting Input ..... –0.3V to VIN + 1.0
A Amplifier Inverting Inputs,
  (Aux. and Normal) ..... –0.3V to VC + 1.0V
Open Collector Output Voltages 20V
A and B Output Currents (Continuous)
  Source ..... Internally Limited
  Sink 1A
Parking Drive (PRKDRV) Output Current
  Continuous 150mA
  Pulsed 1A
Output Diode Current (Pulsed) 1A
Power OK (PWROK) Output Current
  Continuous 30mA
  Pulsed (Note 2) 150mA
Operating Junction Temperature ..... – 55°C to +150°C
Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

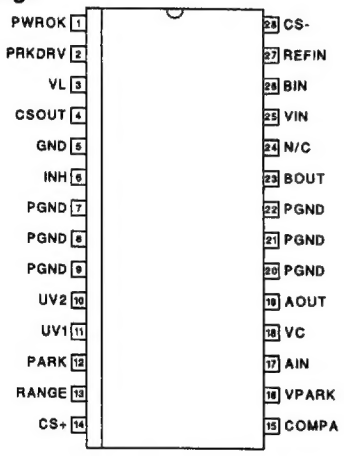
Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.

Note 2: The PWROK output will safely discharge a capacitive load of up to 30 nanojoules.

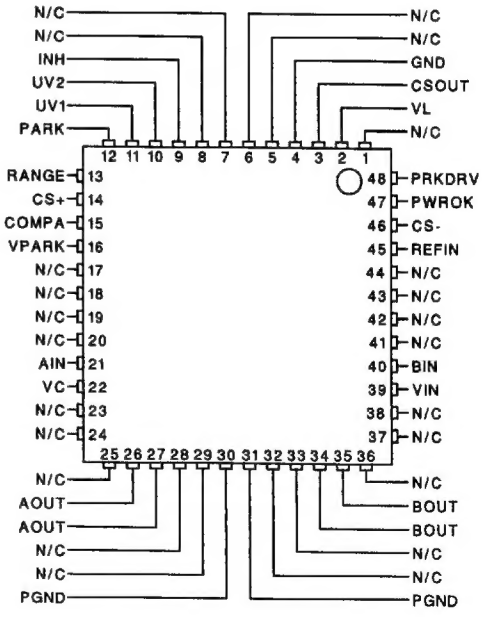
Note 3: Consult Packaging Section of Unitrode Integrated Circuits databook for thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

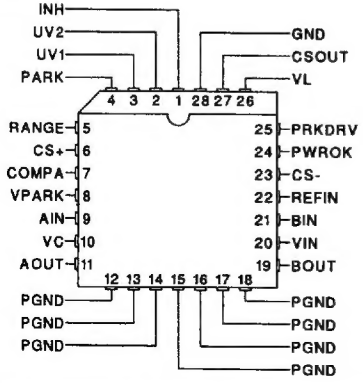
SOIC-28 (Top View)
DWP Package



TQFP-48 (Top View)
FQ Package



PLCC-28 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0 to +70°C, VIN = 5V, VC = VIN = VL, REFIN = VIN/2, RANGE, PARK, and INH = 0V, and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
VIN Supply Current	Low Range Mode		11	15	mA
	High Range Mode		17	23	mA
VC Supply Current	I_{OUT} = 0A, Low Range Mode		1.2	2.5	mA
	I_{OUT} = 0A, High Range Mode		1.2	2.5	mA
VL Supply Current	Low Range Mode		0.75	1.1	mA
	High Range Mode		0.8	1.2	mA
Total Supply Current	Supplies = 5V, I_{OUT} = 0A, Low Range Mode		13	17	mA
	Supplies = 12V, I_{OUT} = 0A, Low Range Mode		14	20	mA
	Supplies = 5V, I_{OUT} = 0A, High Range Mode		19	25	mA
	Supplies = 12V, I_{OUT} = 0A, High Range Mode		21	29	mA
VL UVLO Threshold	Low to High		2.6	2.8	V
UVLO Threshold Hysteresis			200		mV
Under Voltage (UV) Comparator					
Input Bias Current	Max at Either UV Input		–0.25	–1.0	µA
UV Thresholds	Low to High, Other Input = 5V	1.28	1.3	1.32	V
UV Threshold Hysteresis		19	24	29	mV
PWROK Vsat	I_{OUT} = 5mA, UV Input Low		0.15	0.45	V
PWROK Leakage	V_{OUT} = 20V			5	µA
Power Amplifiers A and B					
Input Offset Voltage	A Amplifier, V_{CM} = 2.5V			4	mV
	B Amplifier, V_{CM} = 2.5V			12	mV
Input Bias Current	V_{CM} = 2.5V, Inverting Inputs Only		–150	–500	nA
Input Bias Current at Ref. Input	(REFIN – CS+)/48kohms, T_J = 25°C	15	21	27	µA/V
CMRR	V_{CM} = 1V to 10V, Supplies = 12V	70	90		dB
PSRR	VIN = 4V to 15V, Vcm = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, V_{OUT} = 1V, I_{OUT} = 300mA to V_{OUT} = 10V, I_{OUT} = –300mA	3.0	20.0		V/mV
Gain Bandwidth Product	A Amplifier (Note 4)		3.5		MHz
	B Amplifier (Note 4)		1.0		MHz
Slew Rate	(Note 4)		1.0		V/µs
High-Side Current Limit		1.1	1.6		A
Output Saturation Voltage	High-Side, I_{OUT} = –100mA (Note 5)		0.75		V
	High-Side, I_{OUT} = –300mA (Note 5)		0.85		V
	High-Side, I_{OUT} = –550mA (Note 5)		0.95		V
	High-Side I_{OUT} = –1A (Note 5)		1.15		V
	Low-Side, I_{OUT} = 100mA		0.15		V
	Low-Side, I_{OUT} = 300mA		0.25		V
	Low-Side, I_{OUT} = 550mA		0.3		V
	Low-Side, I_{OUT} = 1A		0.5		V
	Total Vsat, I_{OUT} = 100mA		0.9	1.2	V
	Total Vsat, I_{OUT} = 300mA		1.1	1.4	V
	Total Vsat, I_{OUT} = 550mA		1.25	1.6	V
	Total Vsat, I_{OUT} = 1A		1.65	2.4	V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0 to +70°C, VIN = 5V, VC = VIN = VL, REFIN = VIN/2, RANGE, PARK, and INH = 0V, and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Amplifiers A and B (cont.)					
VC to VIN Headroom	Volts below VIN, delta High-Side, Vsat = 100mV, I_{OUT} = –550mA (Note 5)	0.23	0.4		V
High-Side Diode, V_F	Id = 1A		1.5		V
Low-Side Diode, V_F	Id = 1A, INH Activated, B Amplifier Only		1.5		V
Current Sense Amplifier					
Common-mode Range	Supplies = 12V (Note 4)	–3		13	V
Input Offset Voltage	V_{CM} = 2.5V, Low Range Mode			2.0	mV
	V_{CM} = 2.5V, High Range Mode			4.0	mV
Input Offset Change with Common Mode Input	V_{CM} = 0V to 13V, Supplies = 12V, Low Range Mode			2000	µV/V
	V_{CM} = 0V to 13V, Supplies = 12V, High Range Mode			4000	µV/V
Voltage Gain	V_{DIFF} = +1.0 to –1.0V, V_{CM} = 2.5V, High Range Mode	0.485	0.50	0.515	V/V
	V_{DIFF} = +1.0 to –1.0V, V_{CM} = 2.5V, Low Range Mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, I_{OUT} = 1mA		0.1	0.3	V
	High-Side, I_{OUT} = –1mA, Referenced to VIN		0.1	0.3	V
Parking Function					
PARK Threshold Voltage		0.6	1.1	1.7	V
PARK Threshold Current	Internal Pull-Up, PARK = 0.6V		50	75	µA
PRKDRV Saturation Voltage	I_{OUT} = 50mA		0.15	0.35	V
PRKDRV Leakage	V_{OUT} = 20V			50	µA
Regulating Voltage at VPARK Input		1.275	1.30	1.325	V
Amplifier A Auxiliary Input Bias Current			–300	–750	nA
Amplifier A Parking High-Side Saturation Voltage	I_{OUT} = –50mA, VIN = 0V, VC = VL = 5V, PARK Open, VC to AOUT		0.8	0.95	V
Minimum Parking Supply	At VC and VL, VIN = 0V, AOUT - PRKDRV Vsat > 0.5V, I_{PARK} = 50mA		1.4	1.7	V
Minimum Supply for Parking Drive and Power OK Operation	At VL, VC = VIN = 0V, Vsat < 0.5V, PRKDRV I_{OUT} = 50mA, RI = 30 ohms to 2V		1.1	1.4	V
	PWROK I_{OUT} = 5mA, RI = 300 ohms to 2V		1.2	1.6	V
VL Parking Supply Current	PARK Open, VL = 5V, VC = 1.6V, VIN = 0V, PWROK I_{OUT} = 5mA, PRKDRV I_{OUT} = 50mA		1.6	3.0	mA
Auxiliary Functions					
INH Threshold		0.6	1.1	1.7	V
INH Current	INH = 1.7V		–0.5	–1.0	µA
RANGE Threshold		0.6	1.1	1.7	V
RANGE Current	RANGE = 1.7V		50	100	µA
COMPA Pin Saturation Voltage	RANGE = 0V, Pin Current = ±500µA, Referenced to A_{OUT}		0.02	0.1	V
COMPA Leakage Current	RANGE = 1.7V, Supplies = 12V, A_{OUT} – V_{COMPA} = ±6V			5	µA
Total Supply Current when Inhibited	VIN, VC, and VL currents		1.0	1.8	mA
Thermal Shutdown Temperature	(Note 4)		165		°C

Note 4: Guaranteed by design. Not 100% tested in production.
Note 5: The high -side saturation performance of the UC3172A is referenced to the VIN supply pin. The VC supply pin can operate about 400mV below the VIN supply input without affecting the performance.

PIN DESCRIPTIONS

AIN: Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

AOUT: Output for the A power amplifier, providing one end of the differential drive to the load during normal operation and during park. During a UVLO condition at the VL supply pin, this output is forced to a high, source only state. When the UC3172A is inhibited, this output will be set high, in a source only state.

BIN: Inverting input to the B amplifier. Used to program the gain of the B amplifier to guarantee maximum voltage swing to the load.

BOUT: Output for the B power amplifier, providing one end of the differential drive to the load during normal operation. During park and while inhibited this pin is tri-stated.

COMPA: The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

CS+: The non-inverting input to the current sense amplifier is typically tied to the connection between AOUT and the series current sense resistor.

CS-: The inverting input to the current sense amplifier is typically tied to the load side of the current sense resistor connected in series with the load. This pin can be pulled below ground during an abrupt load current change with an inductive load.

CSOUT: The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

GND: Reference point for the internal reference, UV comparator, and other low-level circuitry.

INH: A high impedance logic input that disables the A and B power amplifiers, as well as the current sense amplifier. The UV comparators and logic functions of the UC3172A remain active. This input has an internal pull-up that will inhibit the device if the input is left open. The INH function is overridden by any condition that forces the park function to be activated.

PARK: Logic input that forces the park condition on the UC3172A. This input has an internal pull-up that will force the park condition if the pin is left open.

PGND: Current return for all high level circuitry, this pin should be connected to the same potential as GND.

PRKDRV: A 100mA drive output that is active low during a park operation. This pin is normally used to supply the low-side drive to the load during parking, in place of the B amplifier. A series resistor can be added between this pin and the load to limit current during park.

PWROK: Indicates with an active low condition that either of the UV inputs are low, or that the supply voltage at the VL input to the UC3172A has dropped below the UVLO threshold. This output will remain active low until the VL supply has dropped to below approximately 1.2V.

RANGE: When this pin is open or at a logic low potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the current sense amplifier will be 2. If this pin is brought to a logic high, the gain of the current sense amplifier will change into its high range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

REFIN: Reference for input control signals to the power amplifier, as well as, the non-inverting inputs to the A and B amplifiers, and the output level shift for the CS amplifier.

VC: High current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A or B amplifiers are activated. This pin can operate approximately 400mV below the VIN supply without affecting the voltage available to the load. This supply pin provides drive to the power amplifiers during a parking operation.

VIN: Provides bias supply to both the power amplifiers and the current sense amplifiers. The high-side drive to the power stages on both the A and B amplifiers is referenced to this pin. The high side saturation voltages are specified and measured with respect to this supply pin. The parking function of the device is fully operational independent of the voltage at this pin.

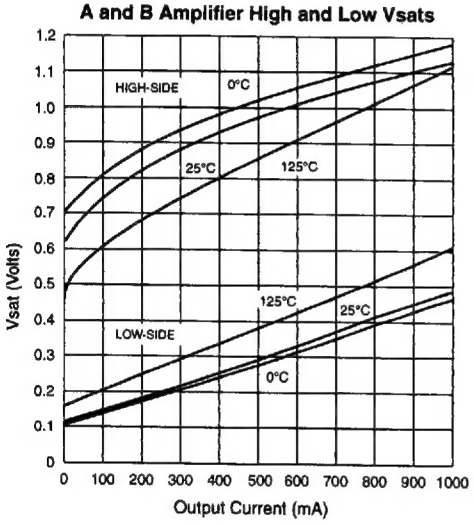
VL: Logic portions of the UC3172A are powered by this supply pin, including the reference, UVLO, the UV comparators, and the PRKDRV and PWROK outputs. This pin is a low current supply that would normally be tied to the VC pin, or to a parking hold up capacitor for extended parking operation with very low recovered back EMF.

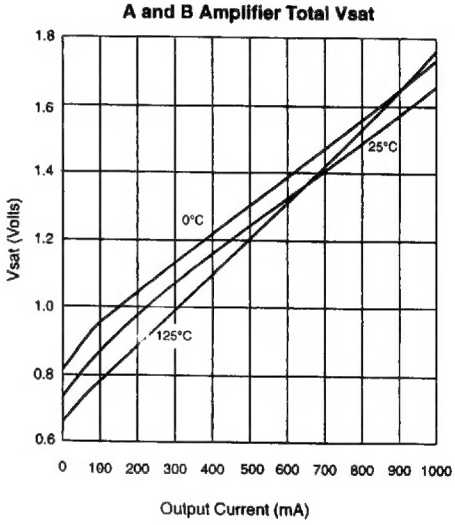
PIN DESCRIPTIONS (cont.)

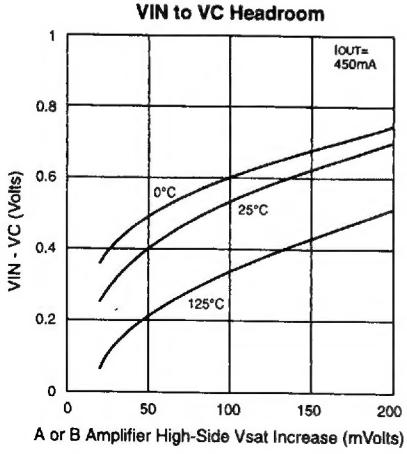
VPARK: The auxiliary inverting input to the A amplifier, activated during park conditions on the UC3172A. An internal auxiliary non-inverting input is connected to the 1.3V reference. When the auxiliary inputs are activated, the A amplifier will force a programmed voltage at its output for a maximum back-EMF/velocity retract of the head. The park condition on the UC3172A is always activated by any one of the following four conditions, 1: a low condition on either of the UV inputs, 2: a high input level at the PARK input, 3: a UVLO condition at the VL supply pin, and 4: activation of the TSD (thermal shutdown) protection circuit. During a UVLO condition at the VL pin the auxiliary inputs to the A amplifier are over-ridden, and the A amplifier output is forced to its high state.

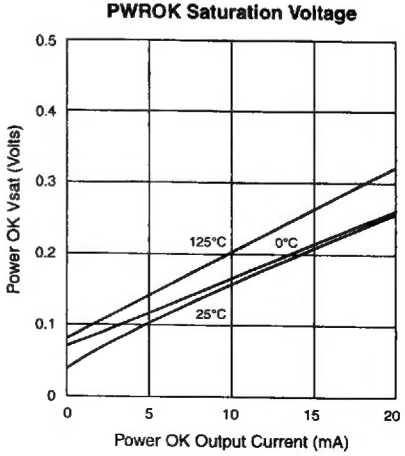
UV1 & 2: Inputs to the UV comparator, these inputs are high impedance sensing points used to monitor external supply conditions. Either of the inputs going low will force the device into a park condition, and force the PWROK output to an active low state. If either of these inputs is not used it should be connected to a voltage greater than 1.3V.

APPLICATION INFORMATION



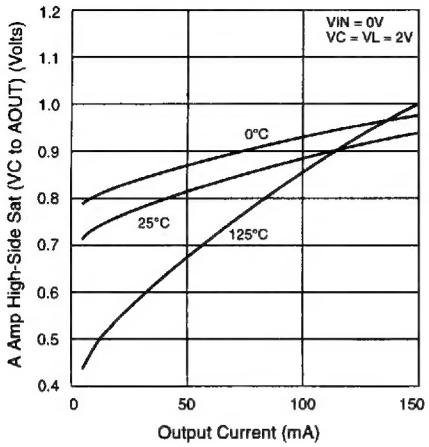




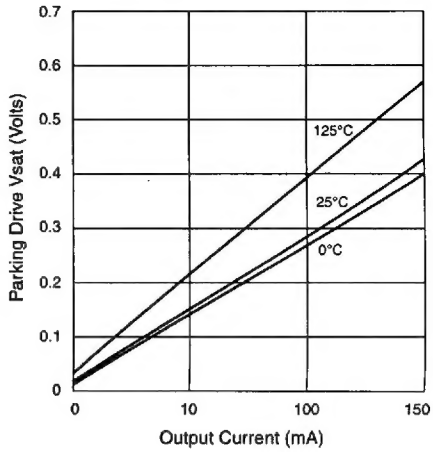


APPLICATION INFORMATION (cont.)

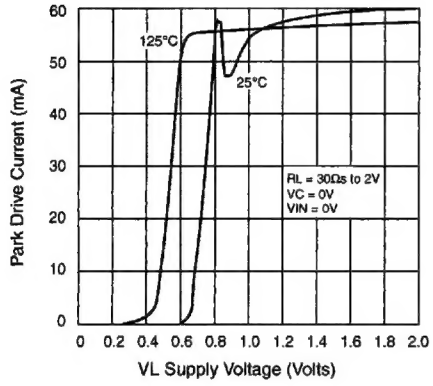
A Amplifier High-Side Vsat in Park Mode



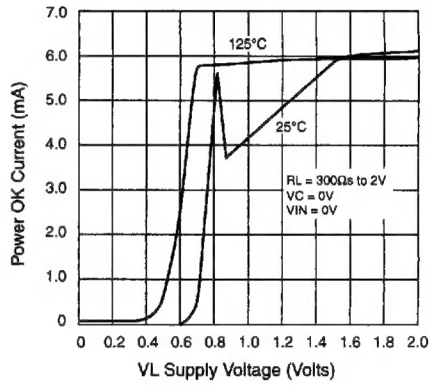
PRKDRV Saturation Voltage



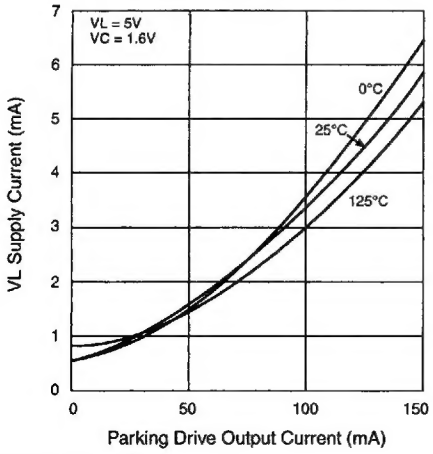
PRKDRV Current vs. VL Supply



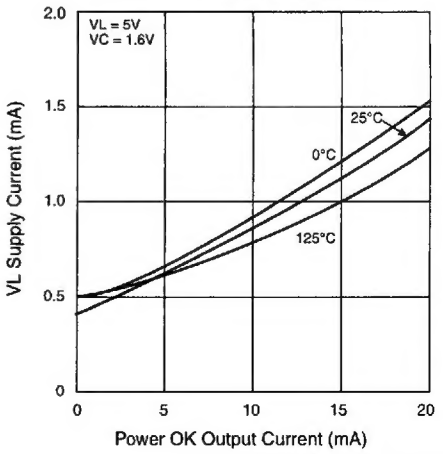
PWROK vs. VL Supply



VL Current vs. PRKDRV Current



VL Current vs. PWROK Current



APPLICATION INFORMATION (cont.)

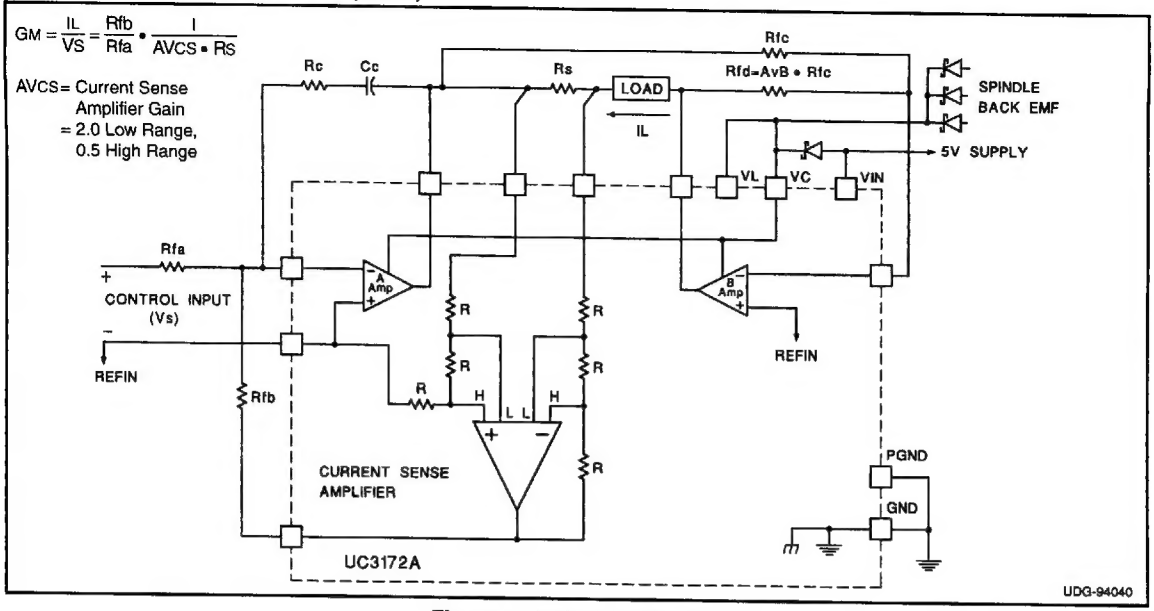


Figure 1. Typical Application

Design Procedure for Application of the UC3172A

The following is a simple design flow that can be used to configure the UC3172A or UC3173A Full Bridge Power Amplifiers as shown in Figure 1.

Definitions:

- f_{3dB} = the closed loop 3dB bandwidth
- A_{VB} = B amplifier closed loop gain, = Rfd/Rfc
- A_{VCS} = current sense amplifier gain, = 0.5 in high range, and 2.0 in low range
- f_{GBWA} = gain bandwidth product of the A amplifier
- G_{MHR} = closed loop transconductance in high range mode
- G_{MLR} = closed loop transconductance in low range mode
- L = load inductance
- R_L = load resistance

A. Choose R_S to be as large as head room will tolerate, this is the series current sense resistor.

B. Choose a value of R_{FB} to be less than the peak current sense amplifier swing divided by 1mA. A value in the range of 3k to 10k is suggested.

C. Calculate R_{FA} according to:

$$(1)\quad R_{FA} = \frac{R_{FB}}{0.5 \bullet R_S \bullet G_{MHR}}$$

If the range change option is not going to be used, it is recommended that the device be set in the low range mode and R_{FA} be calculated by:

$$(2)\quad R_{FA} = \frac{R_{FB}}{2 \bullet R_S \bullet G_{MLR}}$$

D. In order to assure that maximum voltage drive to the load is achievable, there are some precautions that should be taken. In a standard configuration, the B amplifier is slaved to the A amplifier. The bias point of the REFIN and the gain of the B amplifier, as well as the saturation voltages of the power output stages, will affect the voltage available to the load.

There are two simple procedures to follow, either will insure that the capabilities of the device are fully utilized. The first is to set the REFIN voltage at the center of the available voltage swing at the output of the power amplifiers. This optimum reference is defined by equation (3).

$$(3)\quad V_{REF}\ (\text{optimum}) = \frac{VIN - V_{HSsat} + V_{LSsat}}{2}$$

where: V_{HSsat} = high-side Vsat at maximum load
V_{LSsat} = low-side Vsat at maximum load.

A second approach is to raise the gain of the B amplifier to insure maximum swing. For a given REFIN voltage the gain of the B amplifier, set by the ratio of the feedback resistors, can be made greater than unity as given by:

$$(4)\quad A_{VB} = \frac{VIN - V_{HSsat} + V_{REF}}{V_{REF} - V_{LSsat}} \quad \text{or,}$$

$$\frac{V_{REF} - V_{LSsat}}{VIN - V_{HSsat} - V_{REF}}$$

APPLICATION INFORMATION (cont.)

whichever is greater than unity.

For a typical case, where V_{REF} has been set at VIN/2, the required gain for a 5 volt system will be about 1.5, and for a 12 volt system, 1.2.

It is worth noting that when using this method the B amplifier will saturate before the A amplifier on one polarity of the voltage swing. During the time when the B amplifier is saturated and the A amplifier is not, the small signal bandwidth of the loop will be reduced by a factor of (A_{VB} + 1).

E. The normal configuration for compensation of the power amplifier is shown in Figure 1. A simple RC network, $R_C C_C$, around the A amplifier is all that is required.

In the closed loop transconductance amplifier, the A amplifier operates at the highest noise gain. Noise gain is a measure of the feedback ratio at which the amplifier is operating. For the configuration of the A amplifier in Figure 1, the noise gain is given by the impedance ratio of the R_C-C_C series network, to the parallel combination of R_{FA} and R_{FB}. For the A amplifier to operate at its expected closed loop gain, the noise gain at any frequency must not exceed its Gain Bandwidth Product (GBW) divided by that frequency. Applying this to the expression above will yield a result for the maximum 3dB bandwidth that can be achieved for a given configuration.

$$(5)\ f_{3dBmax} = \left(\frac{f_{GBWA} \bullet (1+A_{VB}) \bullet A_{VCS} \bullet R_S \bullet R_{FA}}{2\pi L \bullet (R_{FA}+R_{FB})}\right)\frac{1}{2}$$

In the UC3172A, to accommodate wider power amplifier bandwidths, the f_{GBWA} has been extended to 3.5MHz.

The bandwidth of the closed loop amplifier can be set by choosing the value of R_C. Calculate R_C according to:

$$(6)\ R_C = \frac{2\pi L \bullet f_{3dB} \bullet R_{FB}}{(1 + A_{VB})A_{VCS} \bullet R_S}$$

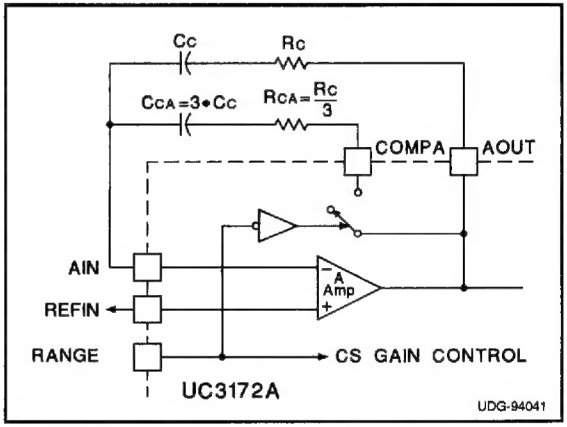
Use A_{VCS} = 0.5 if range changing is to be used, and A_{VCS} = 2.0 if only the low range mode of operation is to be used.

The compensation zero is typically set to coincide with the L/R time constant of the load. C_C can then be calculated by:

$$(7)\ C_C = \frac{L}{R_C(R_S + R_L)}$$

F. When the range change feature of the UC3172A is used, the closed loop bandwidth of the power amplifier will change according to (6). In other words, the bandwidth would be four times larger during the low range mode when A_{VCS} is equal to 2, than during the high range mode when A_{VCS} is equal to 0.5, unless the value of R_C is adjusted to compensate. The COMPA pin on the UC3172A can be used to do this. The COMPA pin acts as a simple switch that allows a parallel compensation network to be applied around the A amplifier during low range operation. A simple network as shown here will keep the loop response constant independent of the range condition.

To maintain the same 3dB bandwidth in both the high and low range modes set R_{CA} and C_{CA} to:



The COMPA pin switches in a parallel compensation network to stabilize the small signal bandwidth with range changes.

$$(8)\ R_{CA} = \frac{R_C}{3},\ C_{CA} = 3C_C$$

Head Parking

In Figure 2, the UC3172A is shown configured to force a programmed voltage at the A amplifier output upon the activation of a park condition. A pair of feedback resistors R1 and R2 set this voltage as defined by:

$$(9)\ R1 = R2\left(\frac{V_{PARK}}{1.3} - 1\right)$$

R2 is typically chosen in the range of 10kΩ to 100kΩ.

The B amplifier output is tri-stated during park, this side of the load is driven low by the PRKDRV pin. A series resistor, RP in the figure, can be inserted in series with the load to limit the peak current if required.

The UV thresholds for the supply monitors are set by picking R4 and R6 values in the 10kΩ to 100kΩ range and then calculating R3 and R5 according to:

APPLICATION INFORMATION (cont.)

(10) $R3 = R4\left(\frac{UV1}{1.3} - 1\right)$, and $R5 = R6\left(\frac{UV2}{1.3} - 1\right)$

During park, supply to the load, and the UC3172A, is typically recovered from the back EMF of the spindle motor. When the supply voltage at the VL supply pin drops below the UVLO voltage, (2.4V high-to-low), the output of the A amplifier is forced high, over-riding the programmed park voltage. The UC3172A will maintain drive to the load down to low supply levels. For example, with 1.5 volts of recovered back EMF, the UC3172A can still deliver 50mA of drive to a 10Ω load.

Parking With Very Low Back EMF

The UC3172A can also be configured to get parking drive to the load with very low recovered back EMF. Figure 3 illustrates how the PWROK pin can be used to drive an external PNP device to achieve very low parking drive Vsat losses. With this configuration, the UC3172A will be able to force approximately one volt across the load with a recovered back EMF voltage of 1.3V.

During system commanded parking with the supplies present, the VPARK pin is still used to set the maximum voltage to the load. The logic function of the PWROK pin is still available since the external PNP will provide isolation to this output when it is high.

Base drive to the PRKDRV and PWROK pins are provided by the VL supply pin. By using a hold up capacitor, CHOLD, the drive can be maintained to the load as the back EMF drops to below 1 volt. A variation on this approach is to add a connection between the VL pin and the recovered back EMF, this will eliminate the need for the holdup capacitor and provide operation down to about 1.2V of back EMF recovery. Care with this approach should be taken in case the 5V supply hangs at just below the programmed UV threshold. In this situation large currents could flow from this supply through the external PNP and into the A output which, until the supply

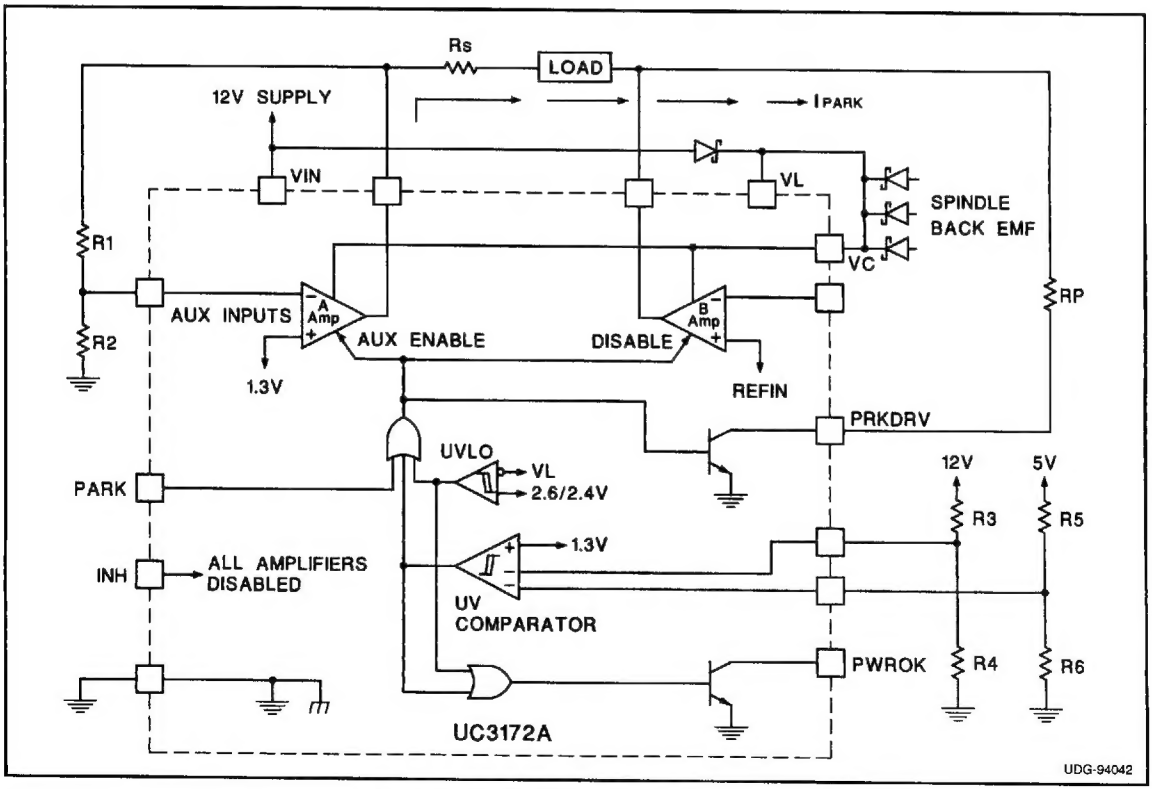


Figure 2. Controlled Velocity Head Parking

APPLICATION INFORMATION (cont.)

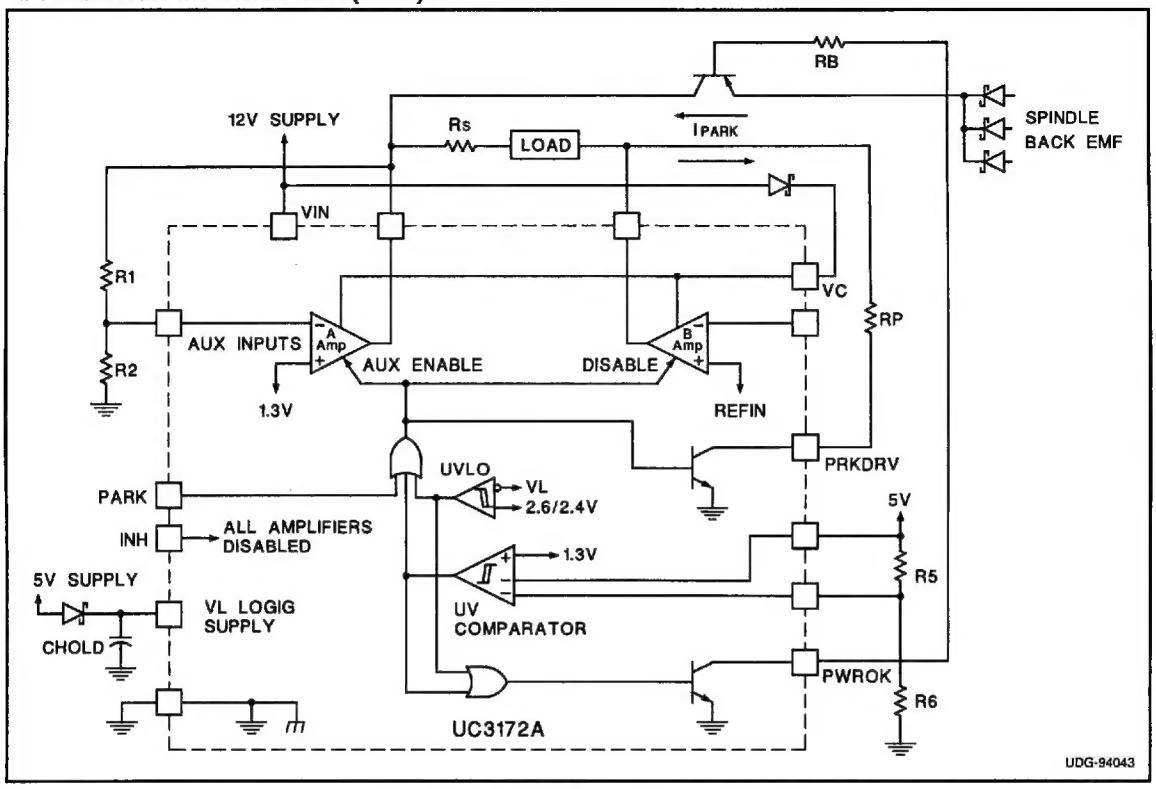


Figure 3. Head Parking with Low Back EMF

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